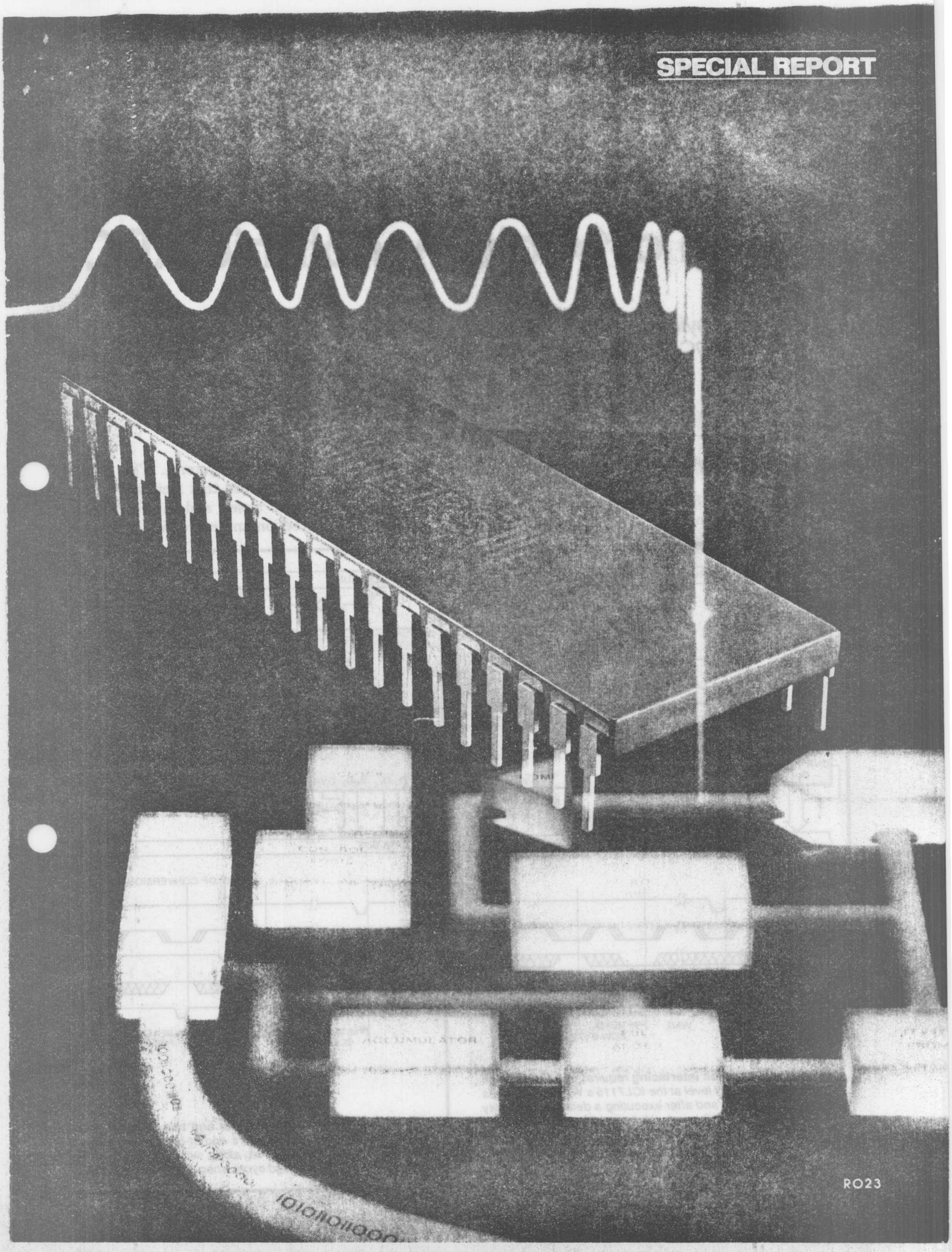
SPECIAL REPORT



Increase analog-system accuracy with a 14-bit monolithic ADC

Employing a unique internal structure, a 14-bit CMOS monolithic ADC improves system performance by providing ±1-LSB accuracy over a broad temperature range and by operating on inputs to 118% of FS.

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Using the ICL7115 monolithic CMOS 14-bit A/D converter, you can design easily calibrated high-resolution data-acquisition systems. The device features an interface structure that facilitates connection to a wide range of μP buses, and an overrange output bit allows the detection and correction of system gain

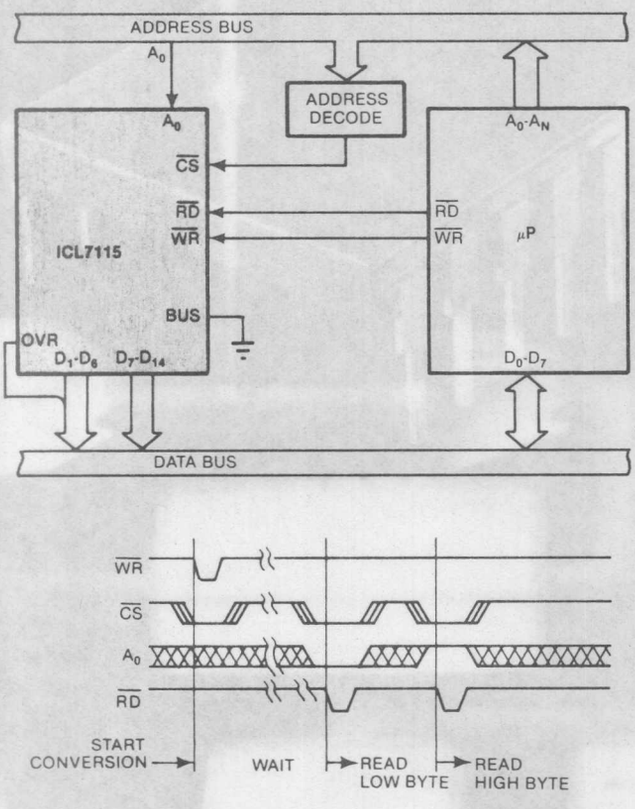

Fig 1—Start-and-wait interfacing *requires minimal external control logic. A LOW level at the ICL7115's WR input initiates a conversion cycle, and after executing a delay loop or utility routine for at least 50 μsec, the host μP reads the ADC's output data in two bytes. When the A_0 line is LOW, the μP reads the LSBs; a HIGH level at A_0 accesses the MSBs and the overrange bit.*

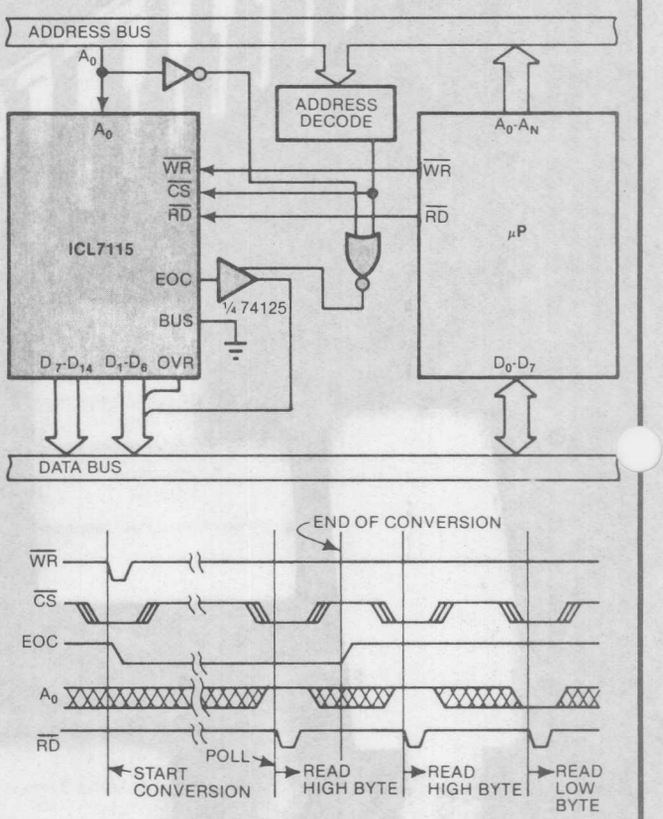

Fig 2—An external 3-state buffer and two control gates *allow a μP to poll the ICL7115's end-of-conversion output. The host reads the EOC bit along with the MSB data, triggering a valid-data-read cycle when the EOC goes HIGH.*

An on-chip PROM holds actual DAC values

errors. Moreover, by providing 14-bit resolution, the ICL7115 lets you eliminate programmable-gain amplifiers from wide-input-range 8- to 10-bit circuits.

The ADC derives its accuracy from an on-chip PROM that holds the actual weighted values of a 17-bit DAC with a radix of 1.85. (For a closer look at the ICL7115's internal operation, see **box**, "14-bit accuracy without laser trimming".) The successive-approximation algorithm based on a 17-bit 1.85-radix converter requires less execution time than a conventional 14-bit base-2 conversion, permitting the ICL7115 to furnish ±1-LSB accuracy with cycle times of less than 50 μsec. And because the ADC's performance depends on PROM values stored after device assembly and accelerated aging, only DAC-ladder temperature tracking, not absolute precision, determines converter accuracy.

Word- or byte-wide outputs

For direct interfacing to 8- and 16-bit μP buses, the ICL7115 provides 3-state output buffers, $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ controls, and bus-control and address inputs. When pulled HIGH, the bus-control circuitry activates

14-bit accuracy without laser trimming

The ICL7115 differs from other 14-bit successive-approximation ADCs. First, its monolithic CMOS construction results in extremely low power consumption—60 mV from ±5V supplies—allowing it to operate from one 5V supply and an ICL7660 voltage inverter.

But this converter's most significant feature is its internal architecture **(Fig A).** Instead of using a conventional 14-bit binary DAC, the ICL7115 employs a 17-bit unit with a radix (exponential base) of 1.85. Thus, the converter accurately measures signals to 118% of full scale and places less weight on the accuracy of DAC-ladder resistors. (The MSB in a binary design, for example, contributes 50% of a full-scale output; the MSB of a 1.85-radix DAC, though, represents only 46% of full scale.)

To ensure accurate conversion despite absolute errors in DAC-resistor values, the ICL7115 employs an error-correction code stored in an on-chip 17×17-bit PROM. Rather than employing theoretical DAC-ladder values in its successive-approximation algorithm, the converter uses PROM-stored measured values obtained after chip fabrication, packaging and artificial aging. Thus, the device requires no trimming, fuse blowing or zener zapping for calibration.

The converter's 14-bit true-binary output code derives from a full-carry adder that accumulates the results of successive-approximation attempts. The adder's final carry output serves as the converter's overflow bit. Ana-

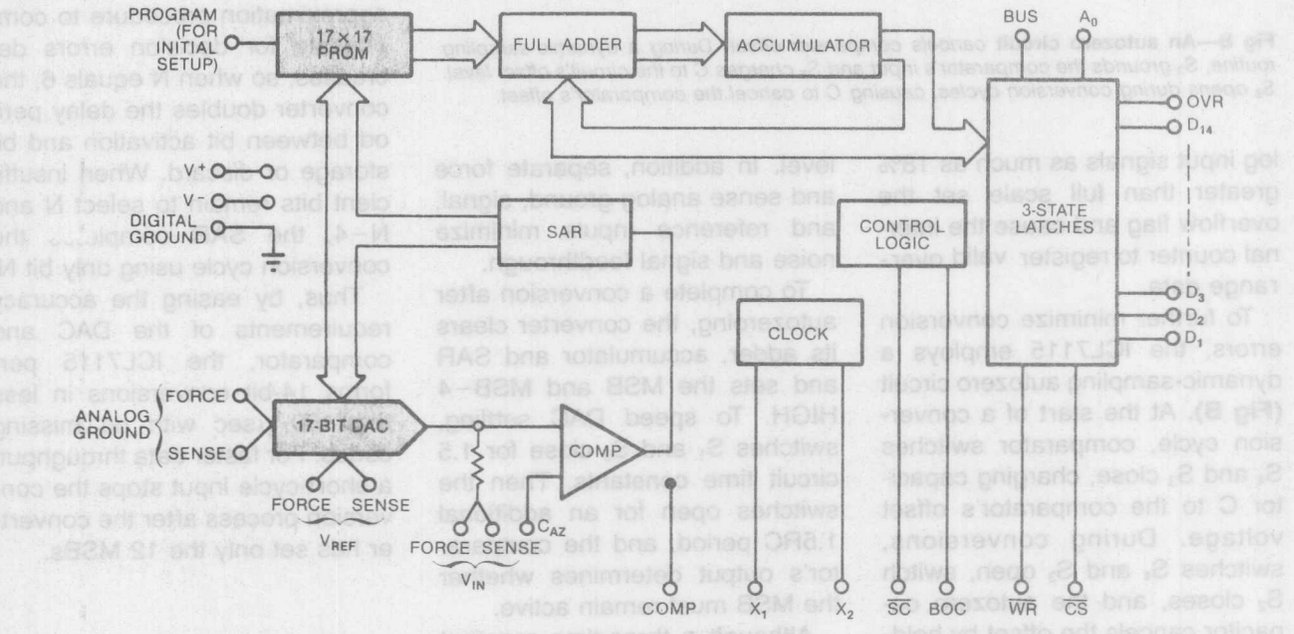

Fig A—Employing an on-chip PROM and a 1.85-radix DAC, *the ICL7115 ADC provides 14-bit resolution with cycle times shorter than 50 μsec. A full-carry adder converts the successive-approximation register's base-1.85 data to true-binary outputs.*

all data output buffers and the overrange (OVR) signal when the $\overline{RD}$ and $\overline{CS}$ lines go LOW simultaneously. Thus, 16-bit μPs can read the converter's output in one instruction cycle.

When the bus-control input is LOW, the state of the converter's address line (A_0) determines which output bits connect to the μP bus. A HIGH level at the A_0 input together with LOW logic states at $\overline{CS}$ and $\overline{RD}$ enable bits D_1 through D_6 and the OVR output; a LOW level at A_0 selects outputs D_7 through D_{14}.

Fig 1 illustrates a typical 8-bit interface, set up for start-and-wait μP control. LOW levels at the converter's $\overline{CS}$ and $\overline{WR}$ inputs, generated by the μP's $\overline{WR}$ line and an I/O- or memory-mapped address decoder, initiate a conversion cycle. After executing a delay or utility routine for a period longer than the ICL7115's conversion time, the processor uses two consecutive bus addresses to read converter output in two bytes.

By adding a 3-state buffer and two control gates, you can use the converter's end-of-conversion (EOC) output to control a start-and-poll μP interface **(Fig 2)**. In this configuration, the A_0 and $\overline{CS}$ lines connect the EOC

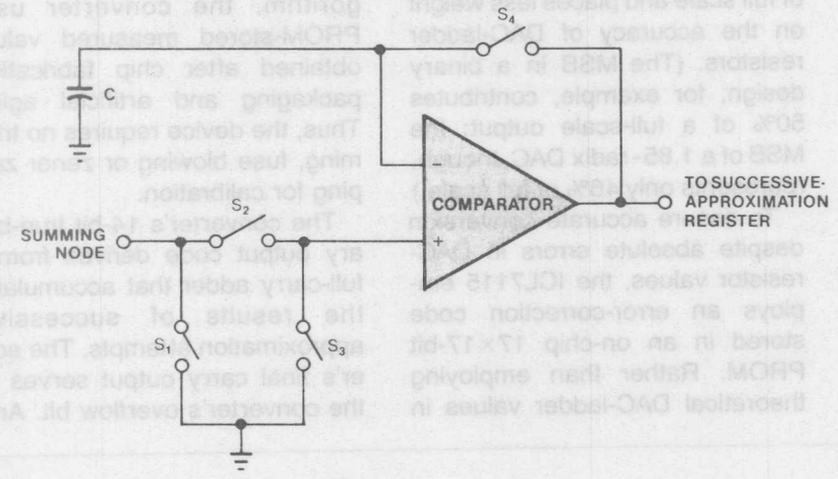

Fig B—An autozero circuit *cancels comparator offset. During a dynamic-sampling routine, S_3 grounds the comparator's input and S_6 charges C to the circuit's offset level. S_6 opens during conversion cycles, causing C to cancel the comparator's offset.*

log input signals as much as 18% greater than full scale set the overflow flag and cause the internal counter to register valid overrange data.

To further minimize conversion errors, the ICL7115 employs a dynamic-sampling autozero circuit **(Fig B)**. At the start of a conversion cycle, comparator switches S_4 and S_3 close, charging capacitor C to the comparator's offset voltage. During conversions, switches S_4 and S_3 open, switch S_2 closes, and the autozero capacitor cancels the offset by holding the comparator's inverting input at the noninverting offset level. In addition, separate force and sense analog-ground, signal, and reference inputs minimize noise and signal feedthrough.

To complete a conversion after autozeroing, the converter clears its adder, accumulator and SAR and sets the MSB and MSB−4 HIGH. To speed DAC settling, switches S_1 and S_3 close for 1.5 circuit time constants. Then the switches open for an additional 1.5RC period, and the comparator's output determines whether the MSB must remain active.

Although a three-time-constant period ensures settling to only 5%, the MSB−4 line, switched ON with the MSB, makes up the difference. If the converter keeps the MSB erroneously, the resulting error cancels when the MSB−4 switches OFF. If the SAR erroneously discards the MSB, the remaining bits, which total 64% of FS, can easily compensate for the mistake.

As the conversion cycle continues, successively diminishing bits N and N−4 switch ON simultaneously. After three time constants, either bit N latches ON or both lines turn OFF. As N becomes increasingly small, the number of bits remaining in the successive-approximation procedure to compensate for decision errors decreases, so when N equals 6, the converter doubles the delay period between bit activation and bit storage or discard. When insufficient bits remain to select N and N−4, the SAR completes the conversion cycle using only bit N.

Thus, by easing the accuracy requirements of the DAC and comparator, the ICL7115 performs 14-bit conversions in less than 50 μsec with no missing codes. For faster data throughput, a short-cycle input stops the conversion process after the converter has set only the 12 MSBs.

output to the data bus along with the high-order-byte data. After beginning a data-acquisition cycle by pulsing the converter's $\overline{WR}$ line, the processor continually reads the converter's high-byte data until it detects a HIGH level on the EOC bit. The start-and-poll interface increases data throughput, compared with start-and-wait schemes, by eliminating delays between conversion-cycle termination and μP-read operations.

Employing alternative interface configurations, you can speed data acquisition without monopolizing the μP for polling operations by using the converter's EOC line as an interrupt generator (**Fig 3a**). Alternatively, you can maximize throughput for sequential conversion cycles by connecting the ICL7115 to a DMA controller (**Fig 3b**).

After you've wired the converter to the μP bus, you must be able to determine if the components in the device's analog input path are properly calibrated. In a 14-bit system, an input gain variation of 0.006% (60 ppm) creates a conversion error of 1 LSB, so to ensure accurate system operation over a wide temperature range, you must be able to measure overall converter gain and correct drift errors. In addition, because 1 LSB in a 14-bit ±5V system corresponds to only 600 μV, you must measure and compensate input offsets.

Conventional data-acquisition systems employ analog multiplexers at their signal inputs to connect a reference voltage to the measurement-signal path. To establish a data-conversion value, the processor reads the known reference level and stores the result. If the system gain exceeds unity, however, the reference overloads the converter's input, resulting in an invalid correction factor. Input references less than the converter's full-scale range permit accurate measurement of input gains greater than one but restrict converter dynamic range.

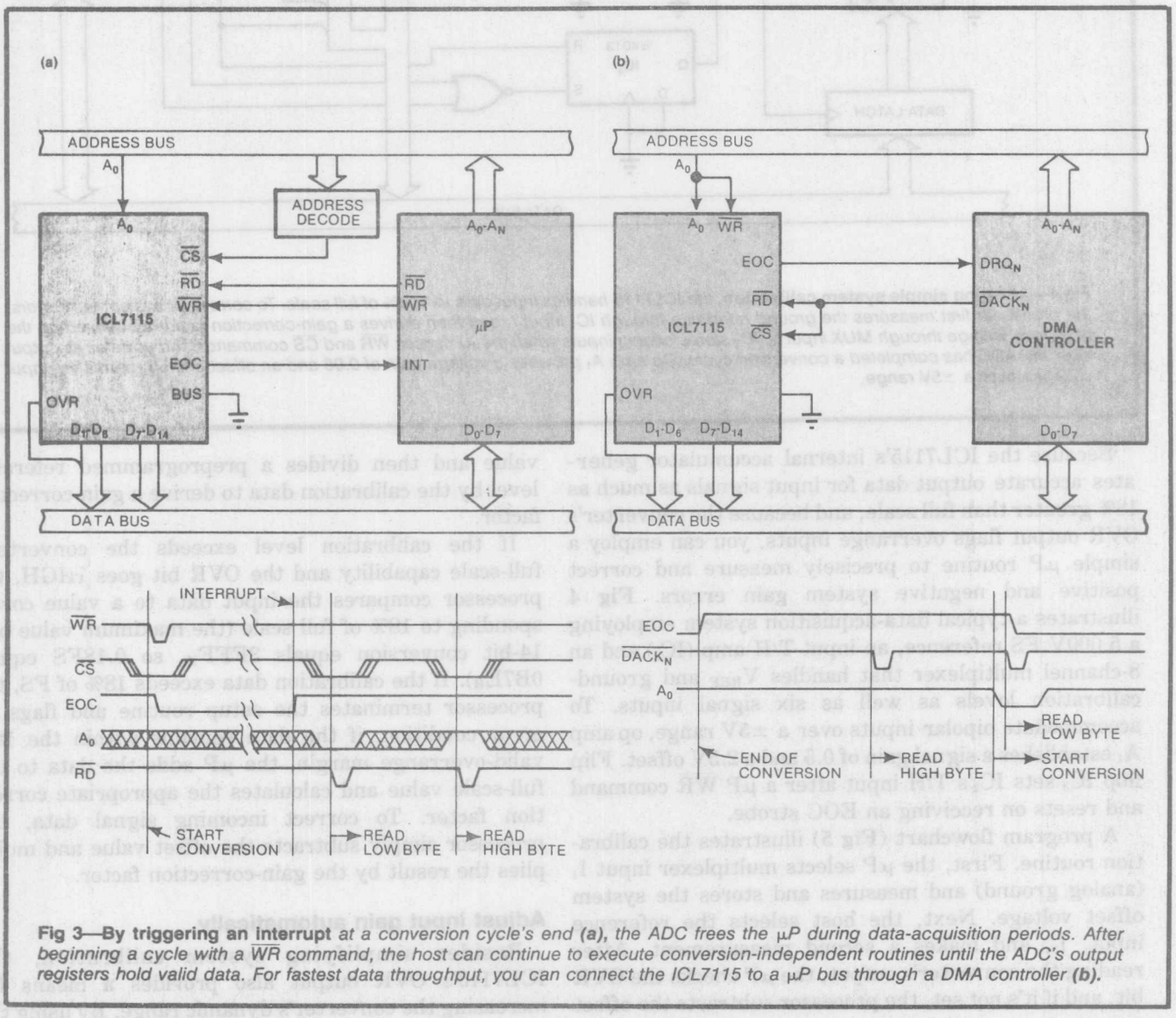

Fig 3—By triggering an interrupt *at a conversion cycle's end* **(a)**, *the ADC frees the μP during data-acquisition periods. After beginning a cycle with a* $\overline{WR}$ *command, the host can continue to execute conversion-independent routines until the ADC's output registers hold valid data. For fastest data throughput, you can connect the ICL7115 to a μP bus through a DMA controller* **(b)**.

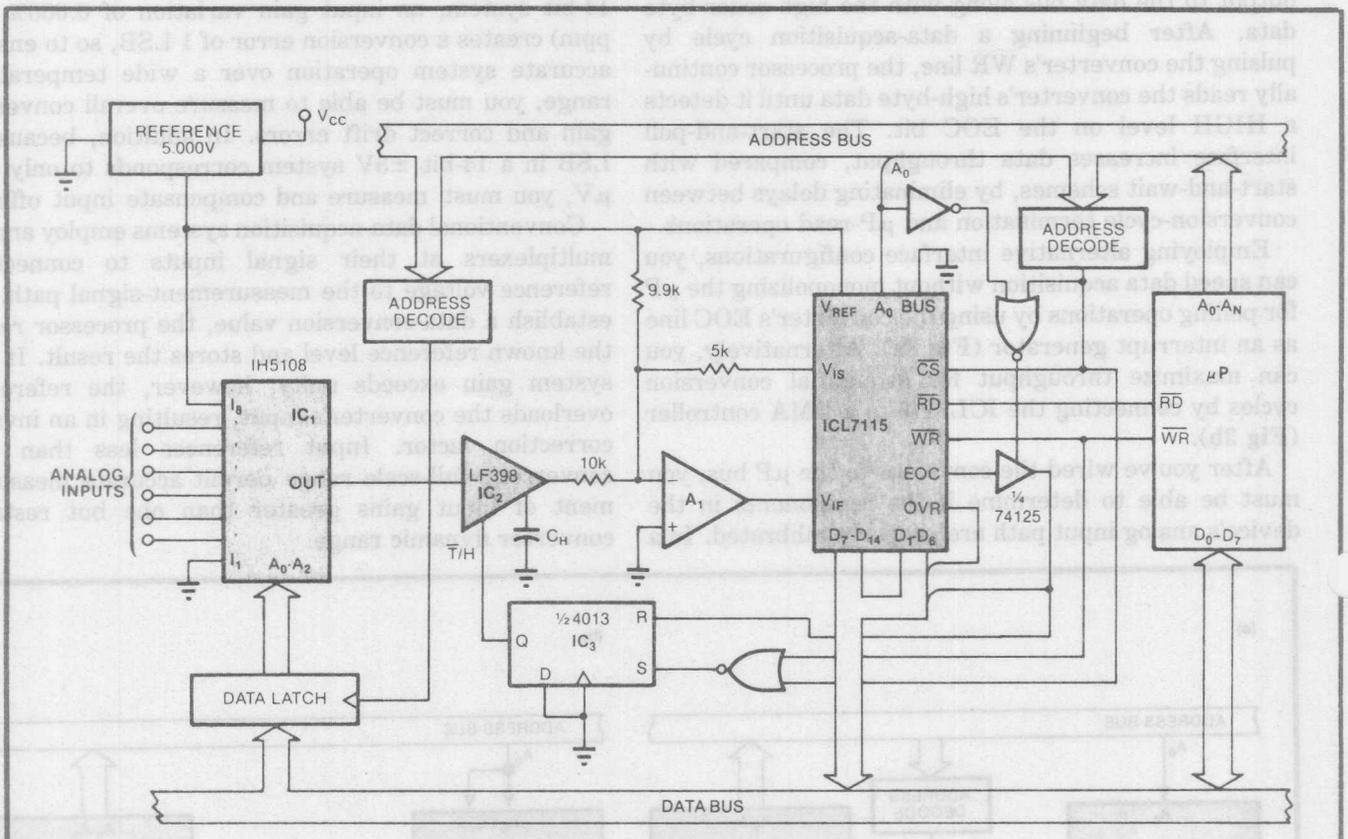

Fig 4—Allowing simple system calibration, *the ICL7115 handles input data to 118% of full scale. To correct for system gain errors, the processor first measures the ground reference through IC_1 input I_1 and then derives a gain-correction factor by converting the reference voltage through MUX input I_8. IC_2 stores analog inputs when the μP issues $\overline{WR}$ and $\overline{CS}$ commands and updates its output after the ADC has completed a conversion cycle. Op amp A_1 provides a voltage gain of 0.05 and an offset of 2.5V, permitting input voltages over a ±5V range.*

Because the ICL7115's internal accumulator generates accurate output data for input signals as much as 18% greater than full scale, and because the converter's OVR output flags overrange inputs, you can employ a simple μP routine to precisely measure and correct positive and negative system gain errors. **Fig 4** illustrates a typical data-acquisition system employing a 5.000V FS reference, an input T/H amp (IC_2) and an 8-channel multiplexer that handles V_{REF} and ground-calibration levels as well as six signal inputs. To accommodate bipolar inputs over a ±5V range, op amp A_1 establishes a signal gain of 0.5 and a 2.5V offset. Flip flop IC_3 sets IC_2's T/H input after a μP $\overline{WR}$ command and resets on receiving an EOC strobe.

A program flowchart (**Fig 5**) illustrates the calibration routine. First, the μP selects multiplexer input I_1 (analog ground) and measures and stores the system offset voltage. Next, the host selects the reference input, I_8, and makes a second measurement. After reading the converter's output, the μP checks the OVR bit, and if it's not set, the processor subtracts the offset value and then divides a preprogrammed reference level by the calibration data to derive a gain-correction factor.

If the calibration level exceeds the converter's full-scale capability and the OVR bit goes HIGH, the processor compares the input data to a value corresponding to 18% of full scale (the maximum value of a 14-bit conversion equals $3FFF_H$, so 0.18FS equals $0B7E_H$). If the calibration data exceeds 18% of FS, the processor terminates the setup routine and flags an error condition; if the data remains within the 18% valid-overrange margin, the μP adds the data to the full-scale value and calculates the appropriate correction factor. To correct incoming signal data, the processor simply subtracts the offset value and multiplies the result by the gain-correction factor.

Adjust input gain automatically

Besides simplifying system calibration, the ICL7115's OVR output also provides a means for increasing the converter's dynamic range. By using the

An overrange output controls input-channel gain

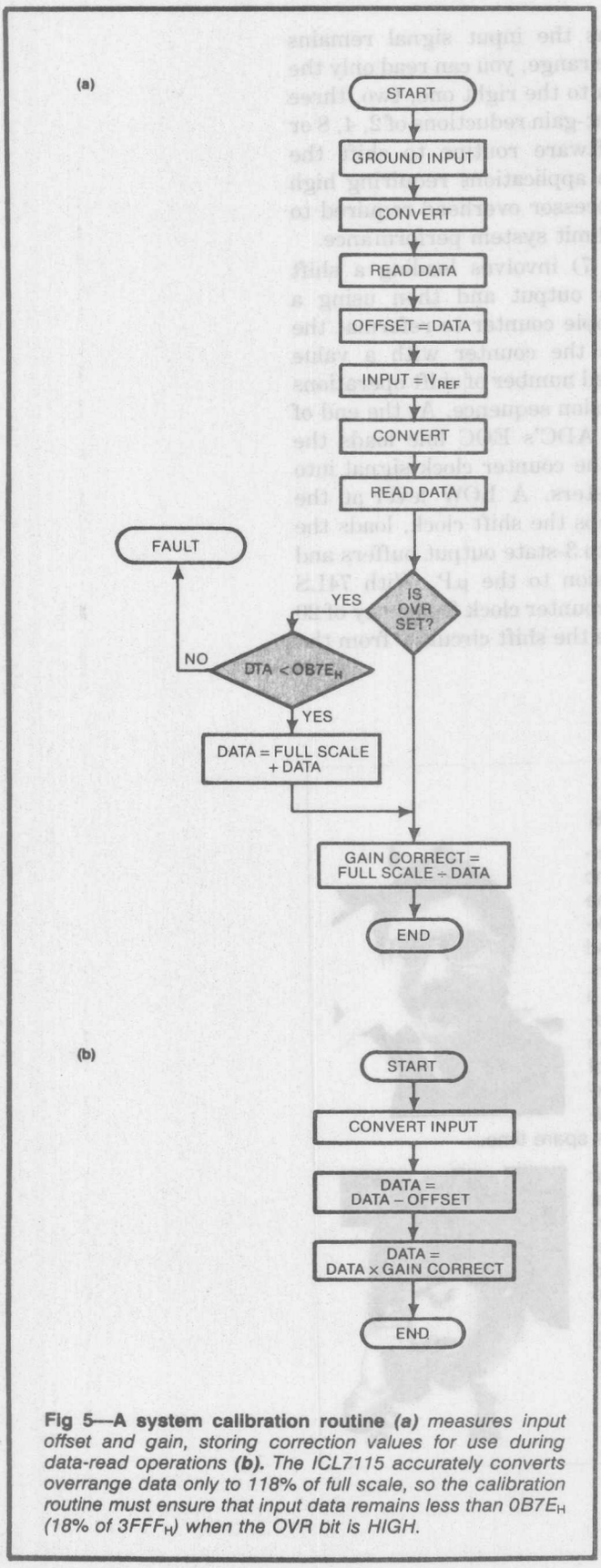

Fig 5—A system calibration routine *(a) measures input offset and gain, storing correction values for use during data-read operations* **(b).** *The ICL7115 accurately converts overrange data only to 118% of full scale, so the calibration routine must ensure that input data remains less than* $0B7E_H$ *(18% of* $3FFF_H$*) when the OVR bit is HIGH.*

overflow bit to control the gain of a programmable-gain amplifier (PGA), you can construct a circuit that selects the maximum allowable signal amplification.

Fig 6 illustrates a self-adjusting conversion system that employs a PGA (A_1) with gains of 2, 4 and 8. A 2-bit counter (IC_1) controls A_1's operation and provides two additional output lines. Thus, by regulating its own input gain, the ICL7115 behaves as a 16-bit ADC.

To begin a conversion cycle, the host μP issues a write command, resetting IC_1. The counter's $\overline{Q_2}$ and $\overline{Q_1}$ outputs go HIGH, selecting a PGA gain of 8, and one-shot IC_2 causes T/H amp A_2 to acquire an input signal. The falling edge of IC_2's Q output triggers the ICL7115's write cycle by driving one-shot IC_3.

If the ADC completes its conversion cycle without registering overrange, the EOC signal, together with a LOW level on the OVR bit, generates a μP interrupt. If the input signal exceeds the ADC's range, the OVR bit sets during the conversion cycle, and the EOC strobe triggers IC_4, advancing the counter and restarting the conversion sequence.

After a conversion attempt using a PGA gain of 4, an OVR output again advances IC_1, but a HIGH level on the counter's Q_2 output ensures an interrupt after the acquisition cycle. If the input remains within the ADC's range during the cycle, the overrange bit remains LOW; a HIGH level on the OVR line clocks the counter, but the interrupt-request signal holds IC_3's enable input LOW, preventing another conversion cycle.

In response to the interrupt, the μP reads the converter system's output by enabling 3-state buffer IC_5 and driving A_0 HIGH, thus selecting bits D_2 through D_6 and the two counter outputs. The μP then checks the counter bits, recording valid data if the states of Q_2 and Q_1 correspond to binary values of 0, 1 or 2 and setting an overrange flag if both counter outputs are HIGH. To complete valid read cycles, the μP accesses the converter's eight LSBs by driving the A_0 line LOW and repeating the read sequence.

To enable the OVR flag during all conversion cycles, a HIGH level on the processor's $\overline{CS}$ line keeps the ICL7115's A_0 input HIGH, and a LOW level on the $\overline{RD}$ input activates the output buffers. Because a 2-byte read cycle allows only two bits for the counter's output, the circuit can employ only three PGA ranges and an overflow flag. You can extend the autoranging converter's capability to four PGA settings by modifying **Fig 6**'s interrupt circuit to trigger after four conversion attempts and by adding the necessary logic to permit the μP to read the ADC's OVR bit directly.

Construct wide-range systems without PGAs

In data-acquisition systems that require wide dynamic range without 14- or 16-bit resolution, you can use the ICL7115 as a medium-resolution converter with an

A 14-bit converter emulates a 10-bit ADC and a PGA

internal PGA. So long as the input signal remains within the ADC's full-scale range, you can read only the 10 LSBs, shifting the data to the right one, two, three or four bits to emulate input-gain reductions of 2, 4, 8 or 16. You can write a software routine to shift the converter's output, but in applications requiring high data throughputs, the processor overhead required to modify data words could limit system performance.

A better method (**Fig 7**) involves loading a shift register with the ADC's output and then using a high-speed clock and a ripple counter to reformat the data. The host μP loads the counter with a value corresponding to the desired number of shift operations and then initiates a conversion sequence. At the end of the conversion cycle, the ADC's EOC line loads the shift registers and gates the counter clock signal into the counter and the registers. A LOW level at the counter's ripple output stops the shift clock, loads the shift registers' contents into 3-state output buffers and signals an end of conversion to the μP. With 74LS Series logic, you can use a counter clock frequency of 20 MHz max, or you can drive the shift circuitry from the ICL7115's clock output. **EDN**

Authors' biographies

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Steve Sockolov is a senior product marketing engineer at Intersil; his duties include marketing and defining data-acquisition products. Employed by Intersil for 1 yr, Steve previously worked for Signetics Corp and earned a BSEE at San Diego State University.

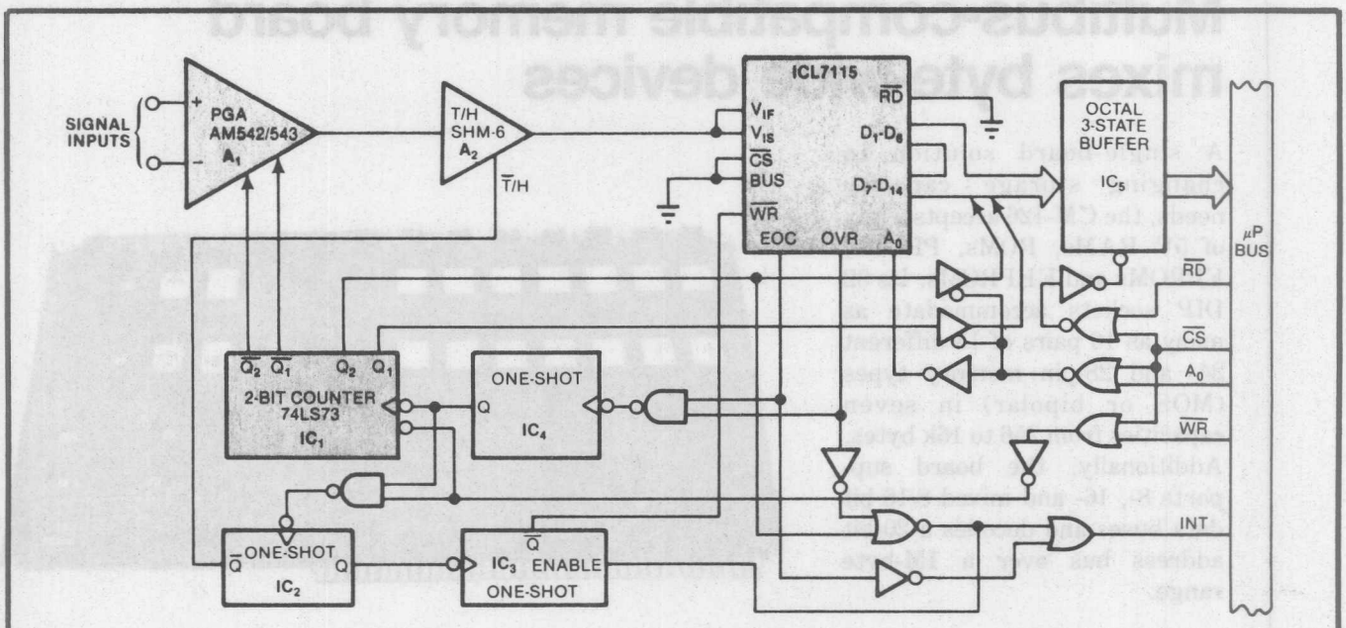


Fig 6—A self-regulating analog input channel, *this circuit employs the ICL7115's overrange output to control the gain of a programmable amplifier A_1. The system begins conversion attempts using A_1's highest gain setting of 8 and sequentially reduces the input amplification until a conversion cycle completes without an overrange or until the counter reaches its maximum output value. The circuit signals a complete conversion by driving the μP's interrupt line HIGH.*

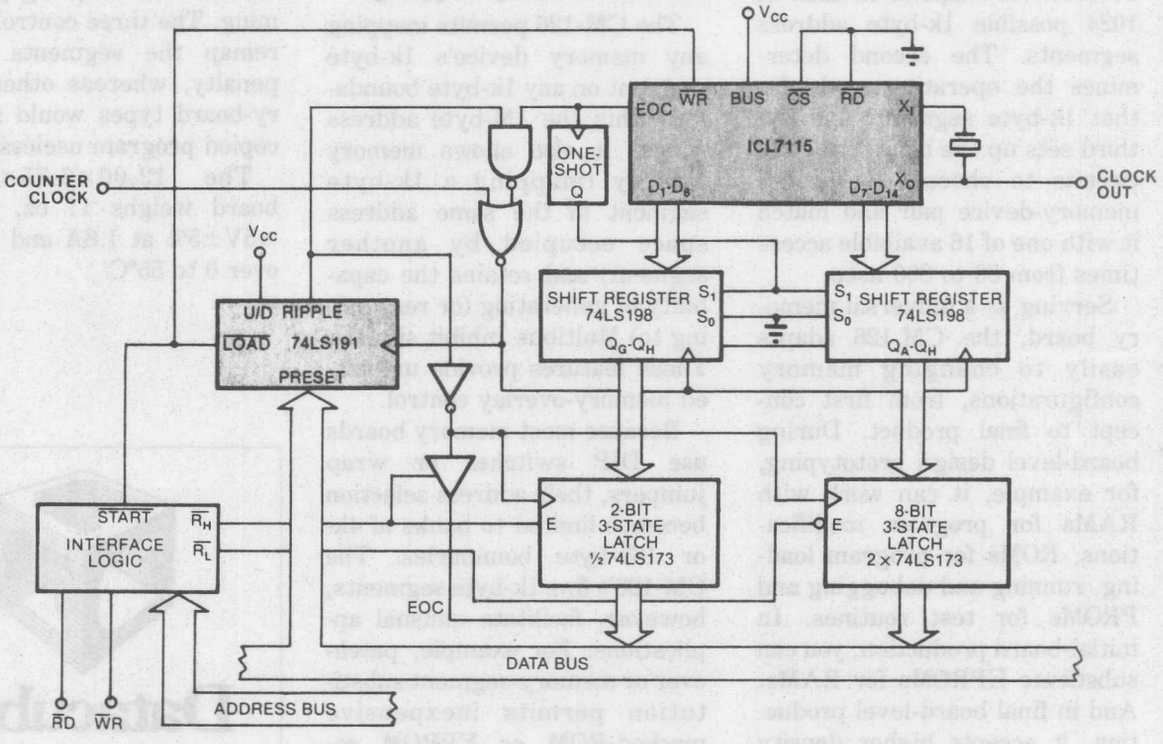
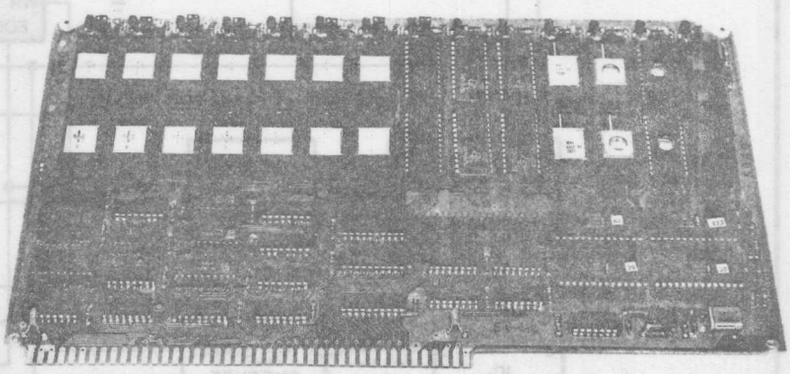


Fig 7—To obtain wide dynamic range *without a programmable-gain amplifier, you can read only the converter's 10 LSBs, shifting data to the right one, two, three or four bits to emulate input gains of ½, ¼, ⅛ or 1/16. The ADC's EOC line loads the shift registers with the conversion data, and the counter clock shifts the data until the ripple counter's output reaches zero. You can use an external counter clock as fast as 20 MHz or drive the shift circuitry from the ICL7115's clock output.*

Multibus-compatible memory board mixes byte-wide devices

A single-board solution to changing storage - capacity needs, the CM-126 accepts a mix of 5V RAMs, ROMs, PROMs, EPROMs and EEPROMs. Its 32 DIP sockets accommodate as many as 16 pairs of 15 different 24- and 28-pin memory types (MOS or bipolar) in seven capacities from 256 to 16k bytes. Additionally, the board supports 8-, 16- and mixed 8/16-bit data buses and decodes a 20-bit address bus over a 1M-byte range.



Providing system access *to as many as 32 RAMs, ROMs, PROMs, EPROMs or EEPROMs in 16 pair combinations, the CM-126 memory board places any mix of 15 generic memory types (MOS or bipolar) on the 8- or 16-bit Multibus.*

3-PROM control

Three on-board programmable bipolar ROMs control the board's memory organization. The first selects which memory devices will respond to each of 1024 possible 1k-byte address segments. The second determines the operating mode for that 1k-byte segment, and the third sets up the board's control circuits to choose the proper memory-device pair and match it with one of 16 available access times from 80 to 800 nsec.

Serving as a universal memory board, the CM-126 adapts easily to changing memory configurations, from first concept to final product. During board-level design prototyping, for example, it can work with RAMs for program modifications, ROMs for program loading, running and debugging and PROMs for test routines. In initial-board production, you can substitute EPROMs for RAMs. And in final board-level production, it accepts higher density EPROMs, bipolar PROMs or masked ROMs, all of different types and speeds.

Versatile memory mapping

The CM-126 permits mapping any memory device's 1k-byte segment on any 1k-byte boundary within the 1M-byte address range. It also allows memory overlay (mapping a 1k-byte segment in the same address space occupied by another segment) and retains the capability of generating (or responding to) Multibus Inhibit signals. These features provide unlimited memory-overlay control.

Because most memory boards use DIP switches or wrap jumpers, their address selection becomes limited to banks of 4k- or 16k-byte boundaries. The CM-126's fine 1k-byte segments, however, facilitate unusual applications. For example, patch-over or memory-segment substitution permits inexpensive masked-ROM or EPROM repairs. Further, some program protection results if you scramble 1k-byte program blocks in random order during programming. The three control PROMs remap the segments without penalty, whereas other memory-board types would render a copied program useless.

The 12.00×6.75×0.50-in. board weighs 11 oz, requires ±5V±5% at 1.8A and operates over 0 to 55°C.

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